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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,481	09/23/2003	Meirav Raz	P-5503-US	9065

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,481	RAZ ET AL.	
	Examiner	Art Unit	
	Paul A. Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Rejection of claim 1 and 4-8 under 35 U.S.C. 112, first paragraph has been rescinded, it is clear through careful examination of applicant's disclosure that "block of bits from which the ECC was not derived" is in reference to the scramble operation and not in reference to another block of bits from a different area of the NVM array (ie. The ECC of block 0 is stored in block 1). The block of bits from which the ECC was not derived in reference to the scrambling function was the interpretation the examiner elected to reject applicant's claims in the first action.

As such, applicant's arguments filed 9 January 2006 have been fully considered but they are not persuasive.

The examiner would like to point out that claim 3 does not have the limitation relied upon by applicant to refute examiner's rejection of pending claims, more specifically that the ECC and data are exclusively drawn from the scrambled or non-scrambled version of the data. Claim 3 states in the preamble that the ECC is derived from the data after it has been scrambled, and states in the second limitation that data is rearranged with an inverse spreading pattern (unscrambled) in order to read a block of bits stored on the NVM. This indicates that both the data and ECC are derived from the scrambled version of data.

The examiner respectfully maintains that Katayama discloses applicant's limitations presented in claim 1,2, 4-7 as relied upon by the examiner in the rejection of said claims. As shown in figure 17, the ECC is performed on the data in its unscrambled

form. The data and generated ECC is then scrambled before being written to the NVM. Since applicant's claims have been presented using the open form of comprising, Katayama's scrambling of the ECC which was derived from the unscrambled data does not teach away from applicant's claimed invention.

Therefore the examiner maintains his rejection of applicant's claims 1-7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al., US PGPUB 2003/0135798.

In regards to Claim 1, Katayama discloses a method of storing bits on a Non-Volatile Memory ("NVM") in figure 17 comprising:

receiving a block of bits in a specific order in element 311;

rearranging the order of the bits in the received block according to a spreading pattern in element 309;

generating an error correction code ("ECC") based on either the original block of bits or based on the rearranged block of bits in element 307; and

storing in said NVM array the ECC and the block of bits in element 303.

Katayama does not disclose that the NVM is an array type of memory; Katayama rather discloses the method is used on optical rewritable disks, which is a linear NVM. Katayama discloses the method is used to extend the number of rewritable times of the memory media in paragraph 13 2nd sentence. Applicant's invention is drawn to scrambling the bits of data stored to a NVM array to reduce the number of errors of the array. It is well known in the art that the primary cause for such errors in an NVM array are due to the limited number of rewrites that can be performed on a memory location of the array. Therefore it would have been obvious to one of ordinary skill in the art to apply Katayama's method of scrambling the bits to an array type NVM in order to extend the number of times the memory can be reliably rewritten.

In regards to claim 2, Katayama discloses a method of reading a block of bits stored in a rearranged order according to a spreading pattern on a Non-Volatile Memory ("NVM") in figure 17 comprising:

rearranging the stored block with an inverse-spreading pattern and manipulating the block with an error correction code ("ECC") generated prior to the block being rearranged according to a spreading pattern and stored in elements 310 and 308.

Katayama does not disclose that the NVM is an array type of memory; Katayama rather discloses the method is used on optical rewritable disks, which is a linear NVM. Katayama discloses the method is used to extend the number of rewritable times of the memory media in paragraph 13 2nd sentence. Applicant's invention is drawn to scrambling the bits of data stored to a NVM array to reduce the number of errors of the

array. It is well known in the art that the primary cause for such errors in an NVM array are due to the limited number of rewrites that can be performed on a memory location of the array. Therefore it would have been obvious to one of ordinary skill in the art to apply Katayama's method of scrambling the bits to an array type NVM in order to extend the number of times the memory can be reliably rewritten.

In regards to claim 3, Katayama discloses a method of reading a block of bits stored on a Non-Volatile Memory ("NVM") in figure 3 along with an error correction code ("ECC"), which ECC is based on the block of bits after being rearranged by a spreading pattern via elements 309 and 307, said method comprising:

rearranging the stored block with the spreading pattern and manipulating the rearranged block with the stored ("ECC") in element 310; and

rearranging the manipulated block of data with an inverse-spreading pattern is inherent since element 310 must perform the inverse function of 309 in order to retrieve the data in its original form.

Katayama does not disclose that the NVM is an array type of memory; Katayama rather discloses the method is used on optical rewritable disks, which is a linear NVM. Katayama discloses the method is used to extend the number of rewritable times of the memory media in paragraph 13 2nd sentence. Applicant's invention is drawn to scrambling the bits of data stored to a NVM array to reduce the number of errors of the array. It is well known in the art that the primary cause for such errors in an NVM array are due to the limited number of rewrites that can be performed on a memory location

of the array. Therefore it would have been obvious to one of ordinary skill in the art to apply Katayama's method of scrambling the bits to an array type NVM in order to extend the number of times the memory can be reliably rewritten.

In regards to claim 4, Katayama discloses a control circuit for storing bits of a data block on a Non-Volatile Memory ("NVM") in figure 17, said circuit comprising:

a bit scrambling block adapted to rearrange the bit of the data block according to a spreading pattern in element 309;

an Error Correction Coding ("ECC") block adapted to generate an ECC based on either the original data block or on the rearranged data block in element 307; and

an NVM storing circuit adapted to store in said NVM array the ECC and the block of bits in element 303.

Katayama does not disclose that the NVM is an array type of memory; Katayama rather discloses the method is used on optical rewritable disks, which is a linear NVM. Katayama discloses the method is used to extend the number of rewritable times of the memory media in paragraph 13 2nd sentence. Applicant's invention is drawn to scrambling the bits of data stored to a NVM array to reduce the number of errors of the array. It is well known in the art that the primary cause for such errors in an NVM array are due to the limited number of rewrites that can be performed on a memory location of the array. Therefore it would have been obvious to one of ordinary skill in the art to apply Katayama's method of scrambling the bits to an array type NVM in order to extend the number of times the memory can be reliably rewritten.

In regards to claim 5, Katayama discloses reading circuit adapted to read a stored block of bits from the NVM array in element 304.

In regards to claim 6, Katayama discloses a de-scrambler adapted to rearrange a block of bits stored according to spreading pattern in element 310.

In regards to claim 7, Katayama discloses the ECC block is adapted to manipulate the de-scrambled block of data according to an ECC which is based on the original data block prior to scrambling in elements 307-309.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

8/6/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER